

SWITCH WITH LINECARDS AND SWITCHING FABRIC

FIG. 1

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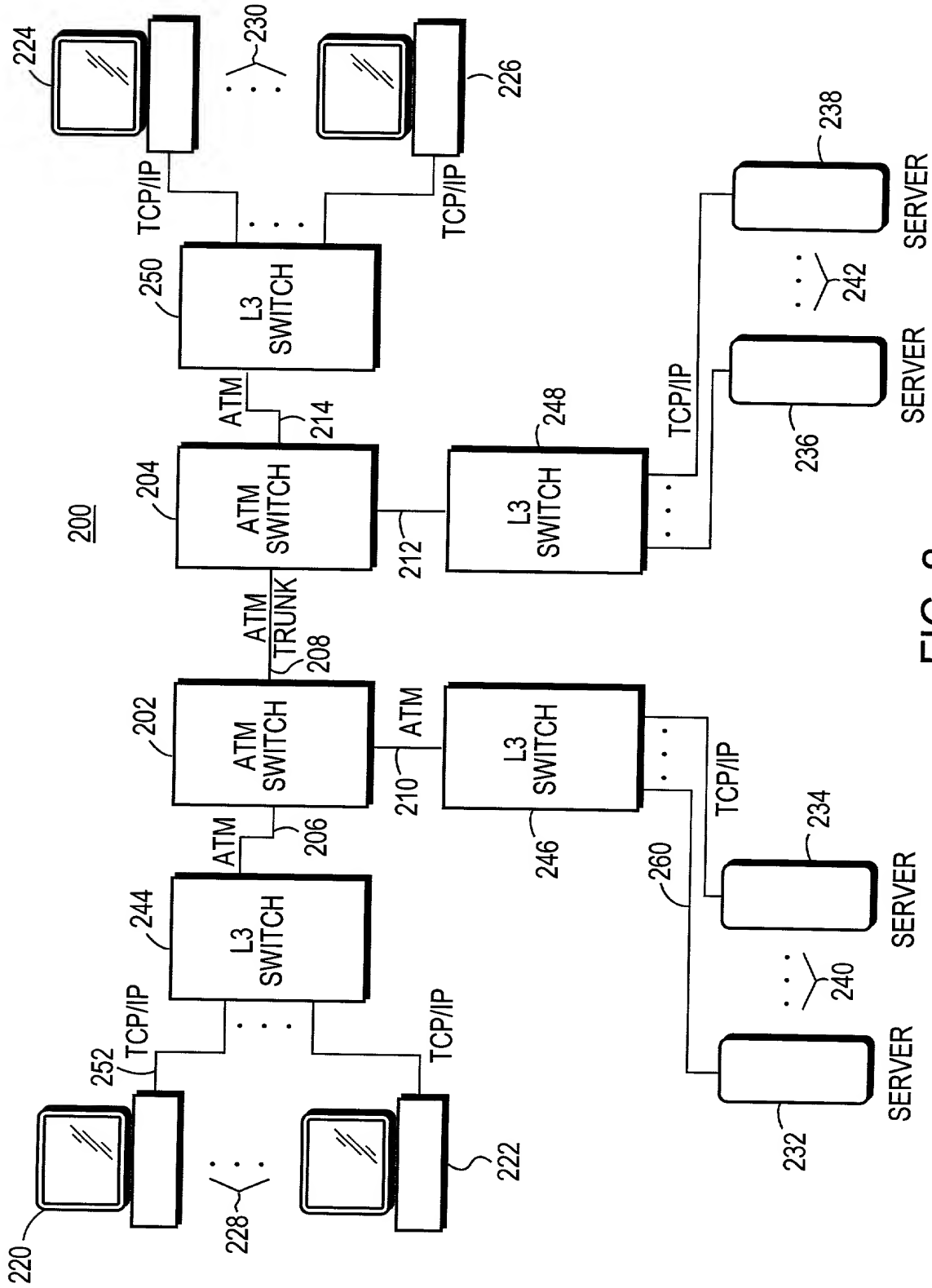
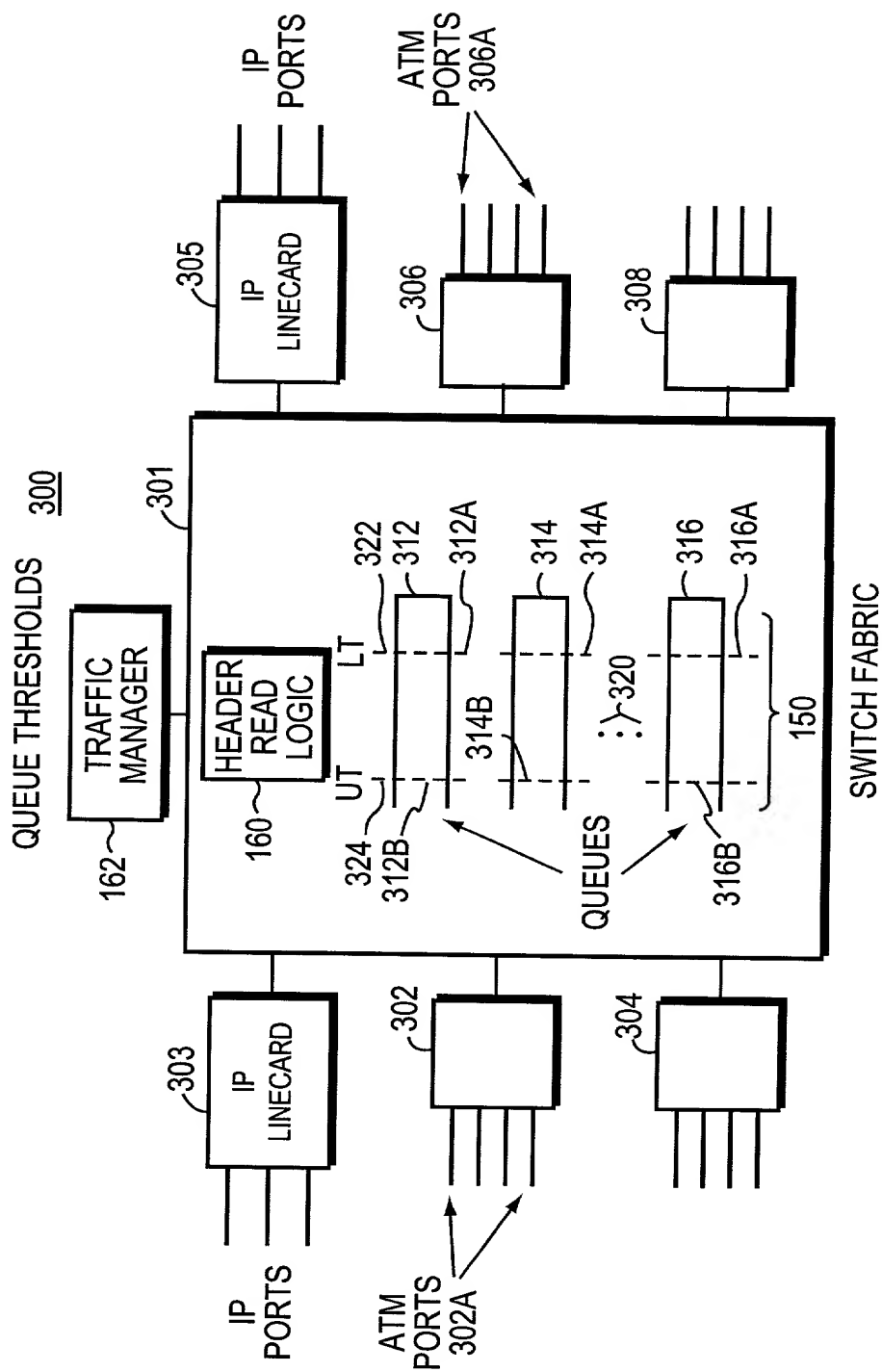


FIG. 2

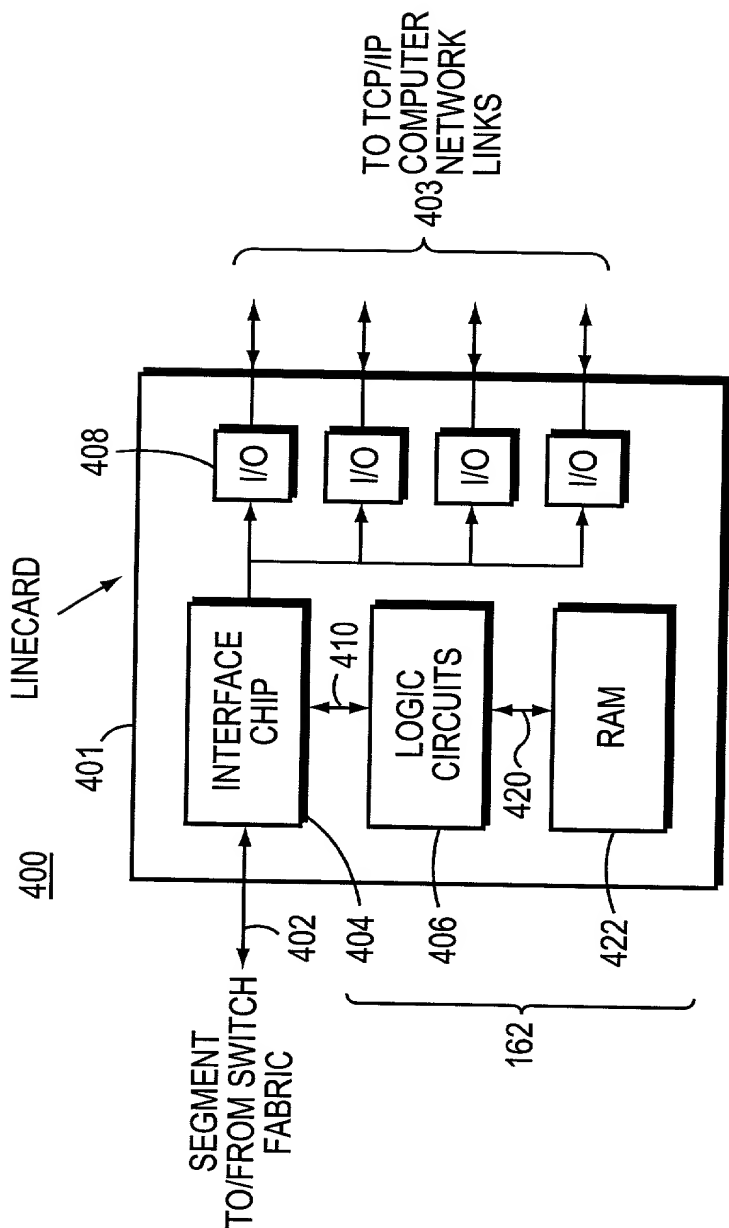
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SWITCH FABRIC WITH LINECARDS, QUEUES AND THRESHOLDS

FIG. 3



LINECARD WITH LOGIC CIRCUITS FOR EXECUTING RED ALGORITHM,
RAM MEMORY FOR STORING DATA

FIG. 4

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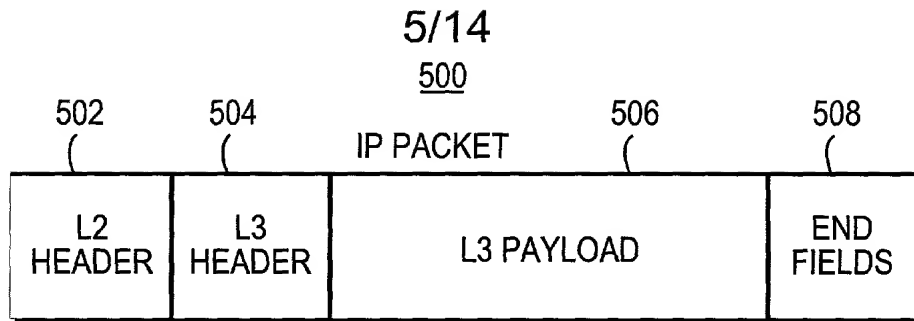


FIG. 5

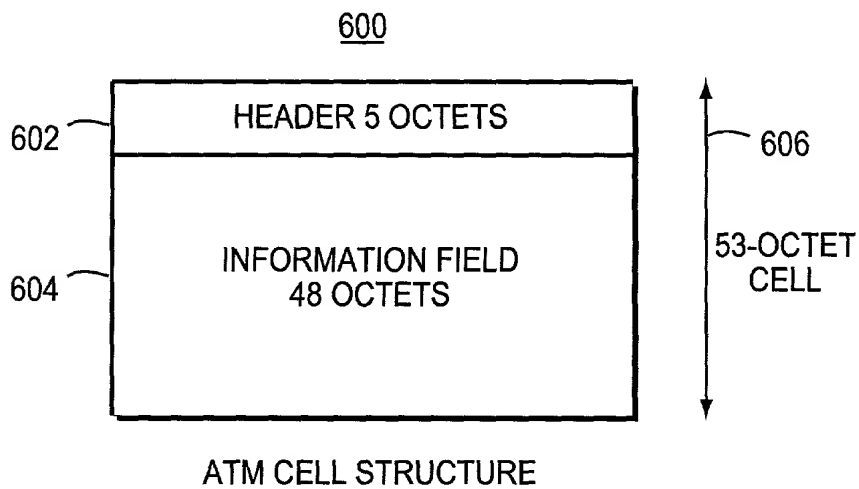


FIG. 6

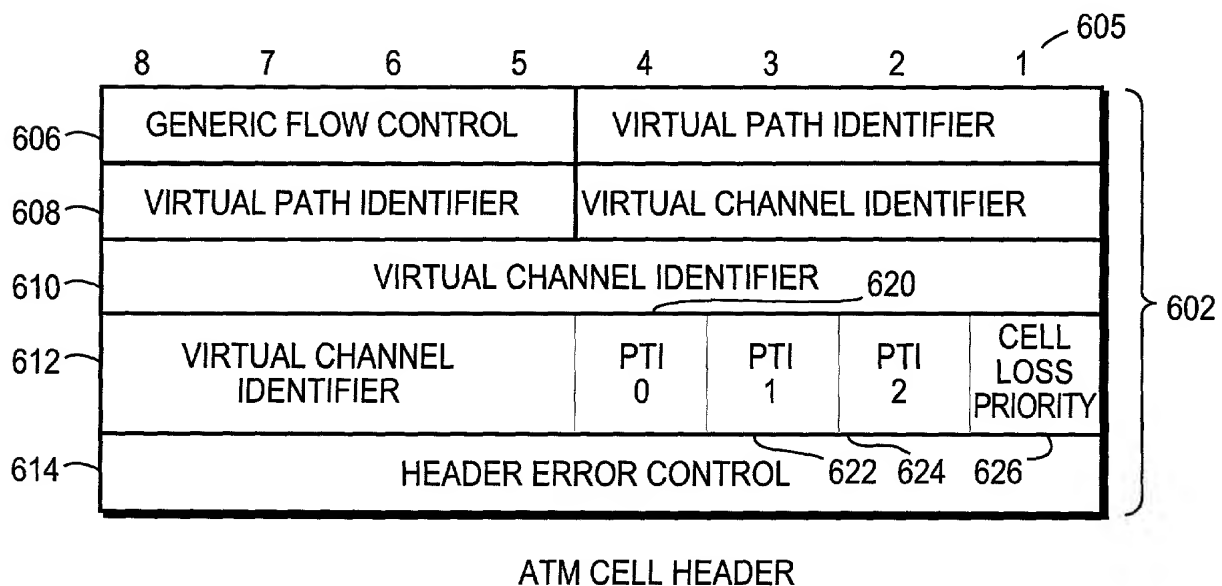


FIG. 7

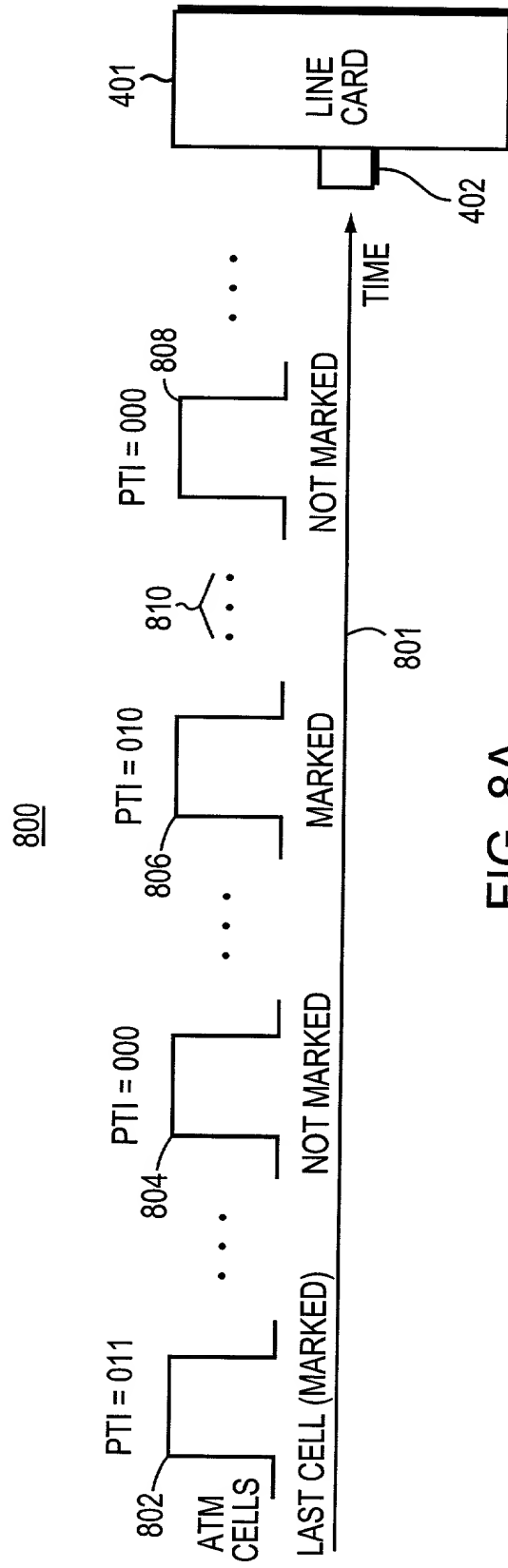


FIG. 8A

ATM RED VC STATE DIAGRAM

820

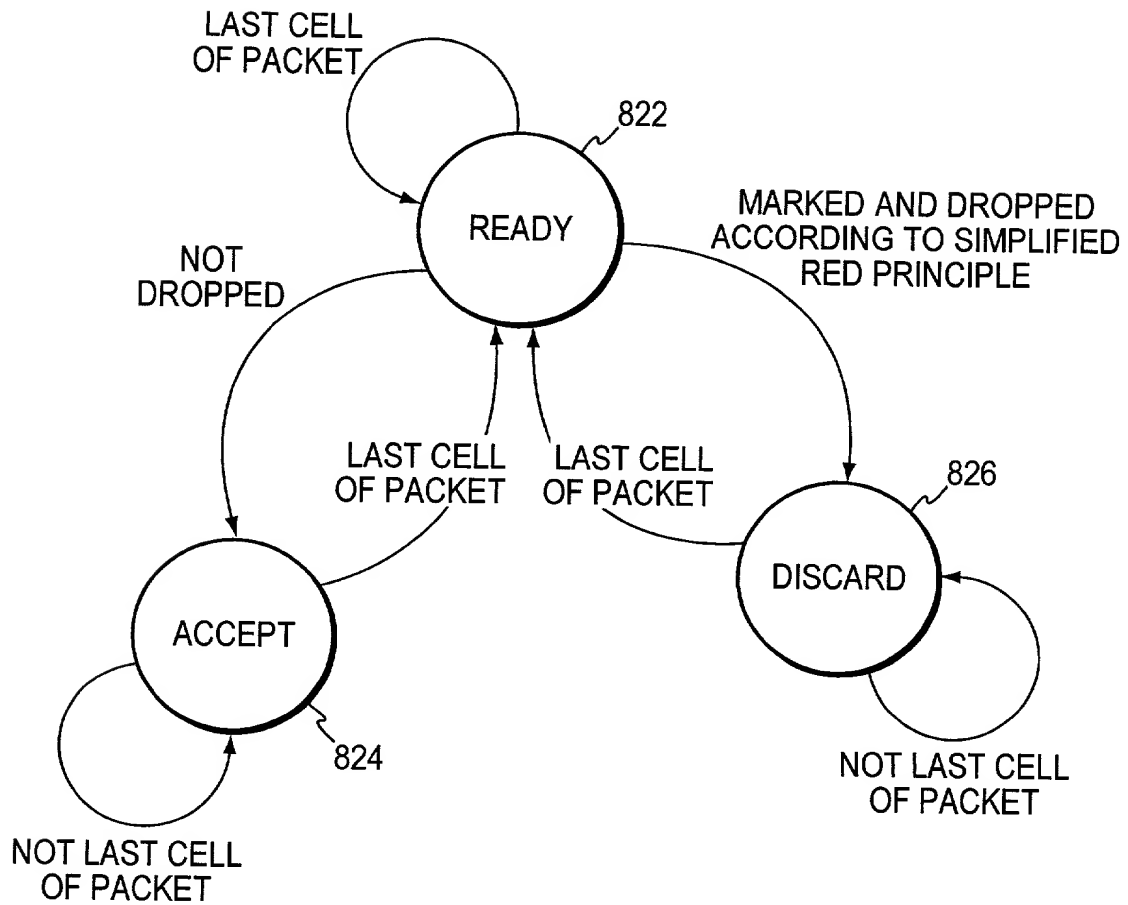


FIG. 8B

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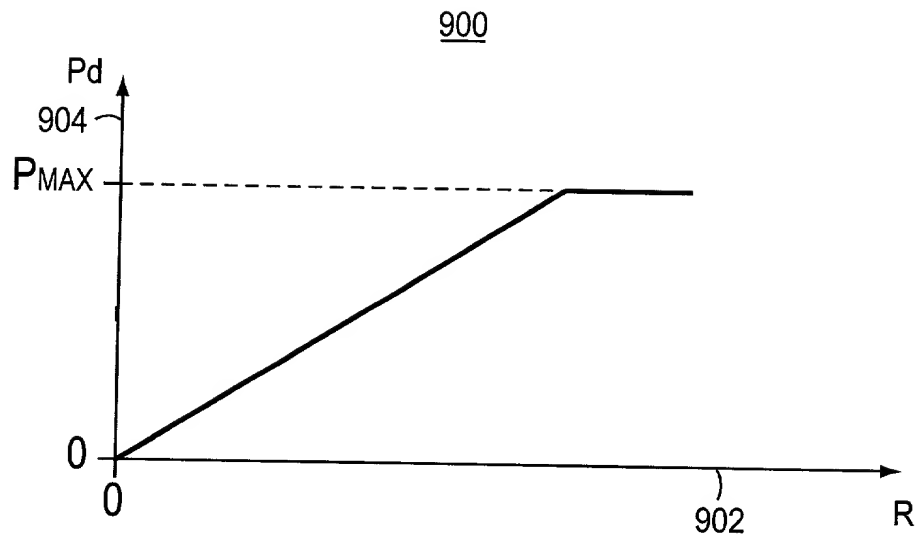


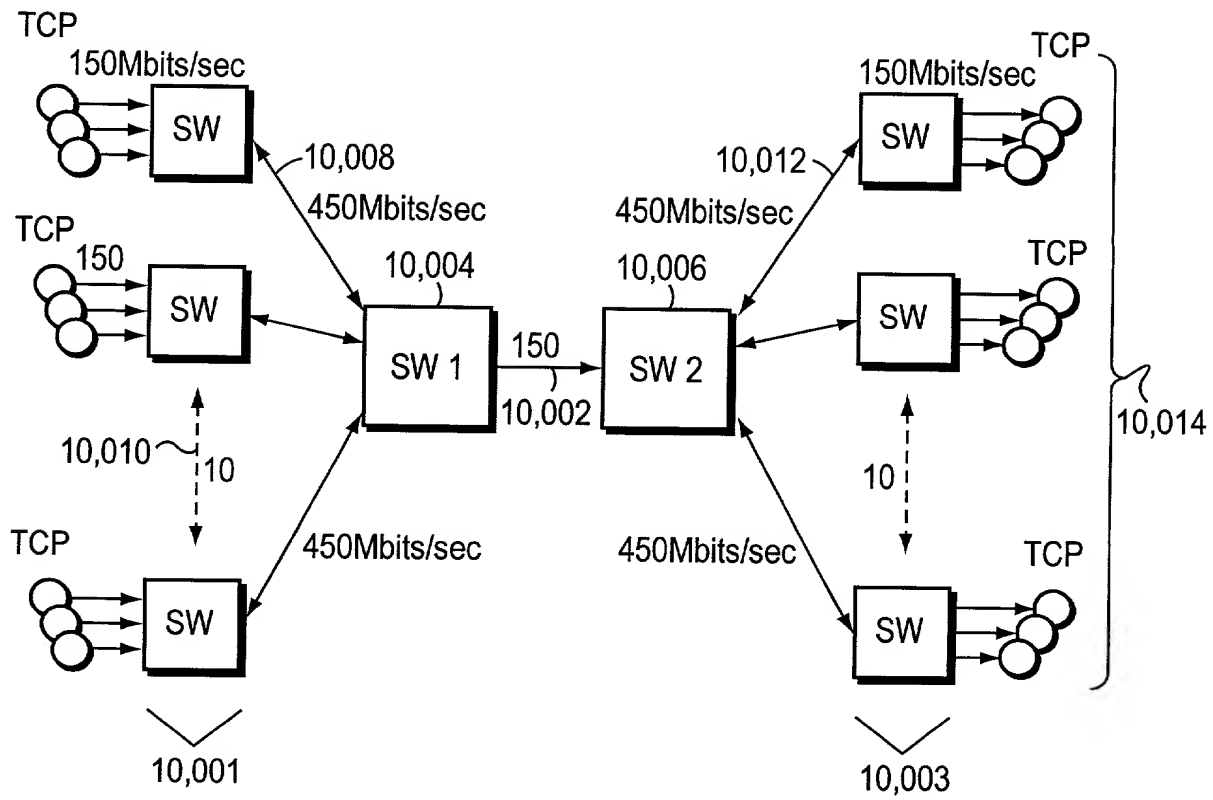
FIG. 9

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0924078.030204
102080" 82012560

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TOPOLOGY FOR RED SIMULATIONS

FIG. 10

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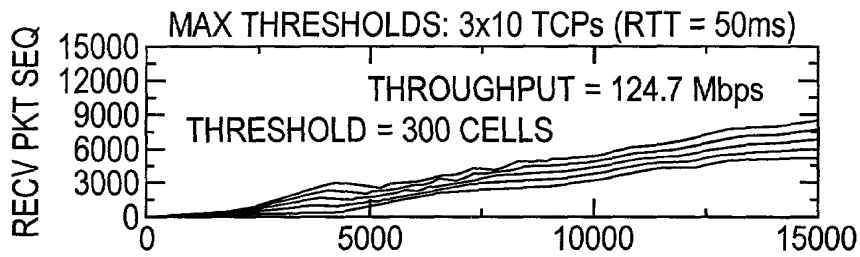


FIG. 11A

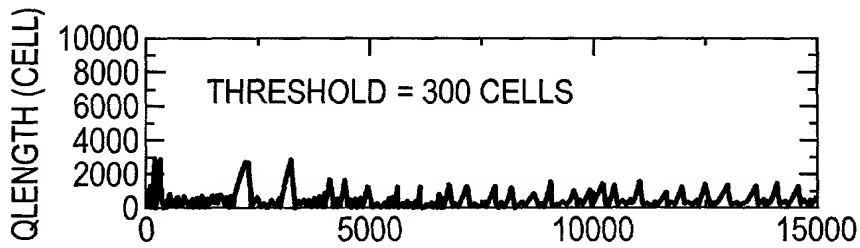


FIG. 11B

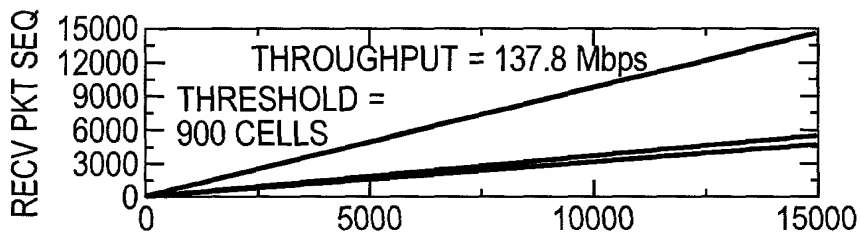


FIG. 11C

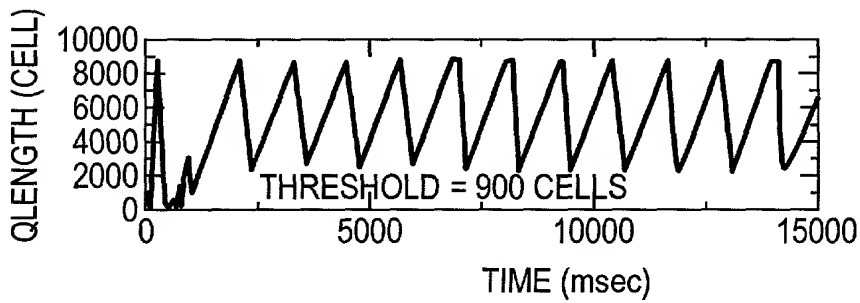
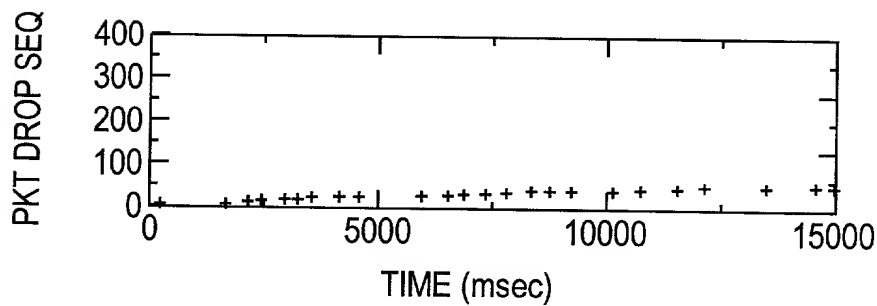
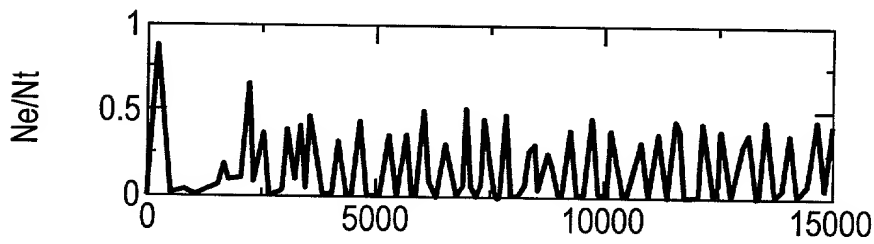
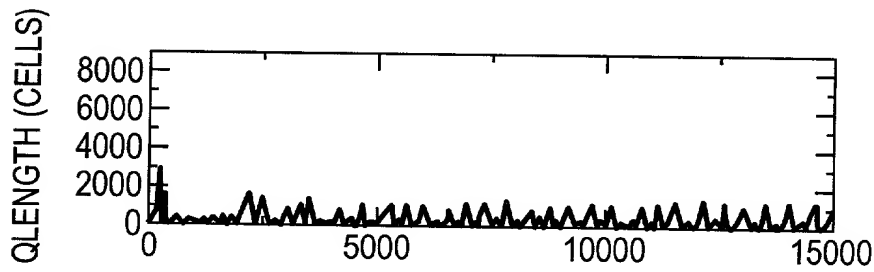
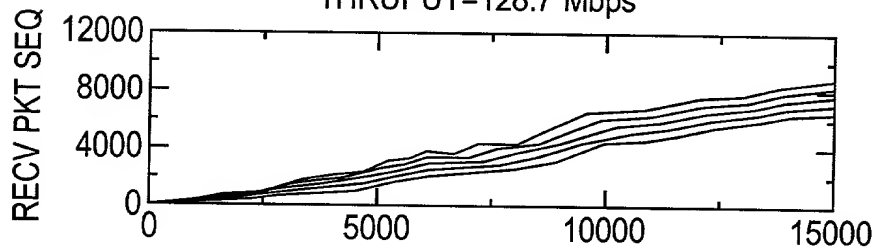


FIG. 11D

RESULTS FOR EPD-THRESHOLD = 300, 900

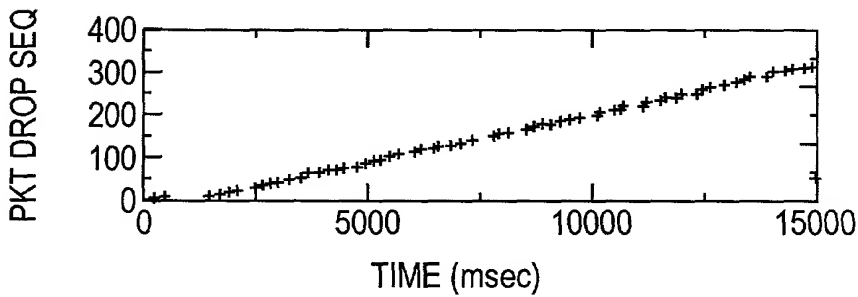
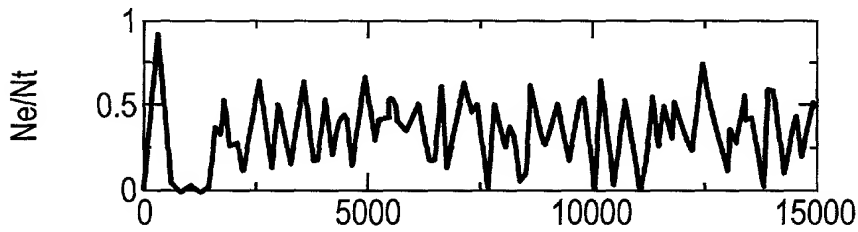
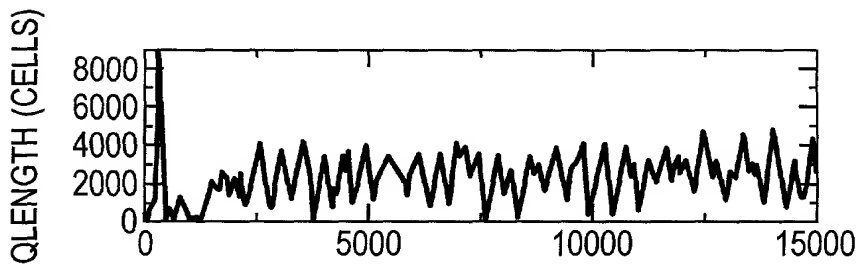
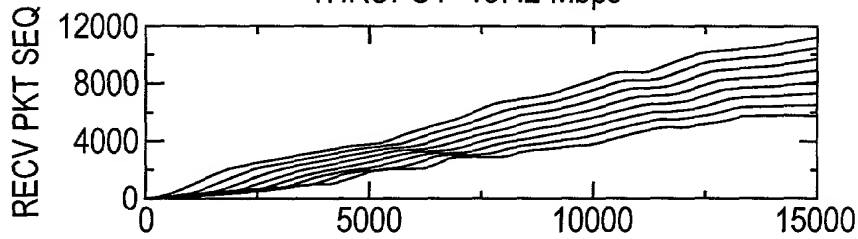
RED: 3x10 TCPs (RTT = 50ms)
Qth=100/300; MAXP=0.01; FREEZE=100ms;
THRUPUT=128.7 Mbps



RESULTS FOR EFCI-THRESHOLD = 100,
EPD = 300

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RED: 3x10 TCP (RTT = 50ms)
Qth=300/900; MAXP=0.01; FREEZE=100ms;
THRUPUT=137.2 Mbps



RESULTS FOR EFCI-THRESHOLD = 300,
EPD = 900

RED: 3x10 TCP (RTT = 50ms)
 Qth=300/900; MAXP=0.01; FREEZE=200ms;
 THRUPUT=137.3 Mbps

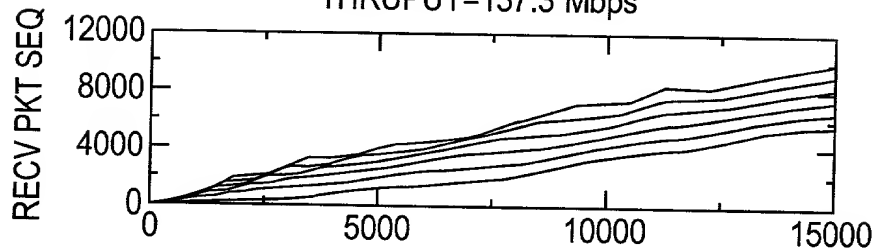


FIG. 14A

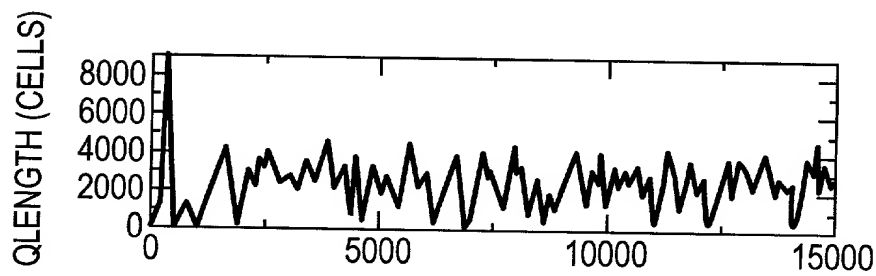


FIG. 14B

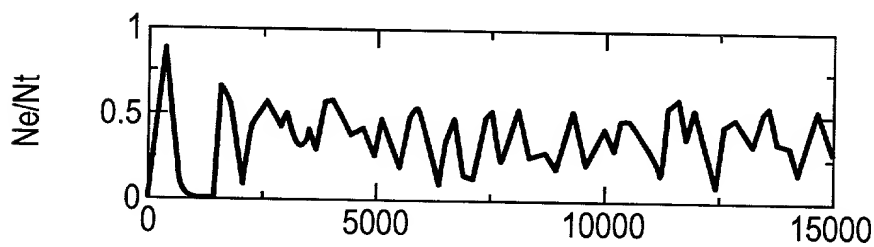


FIG. 14C

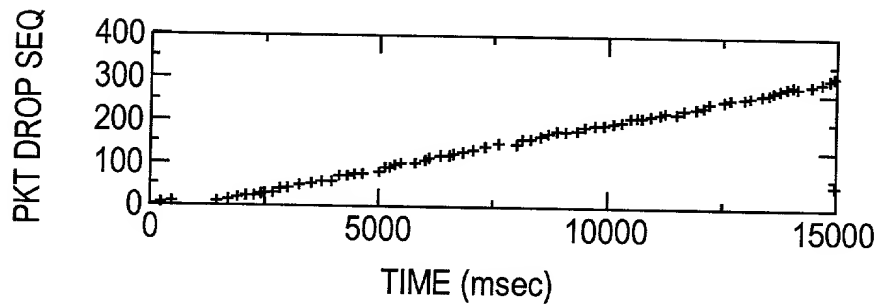


FIG. 14D

RESULTS FOR PD UPDATE INTERVAL = 200 msec

RED: 10/20 (Hi/Lo) TCPs (RTT = 50ms)
 PER-CLASS VS. PER-CLASS PER-PREF RATIOS; MAXP=1.0/2.0%

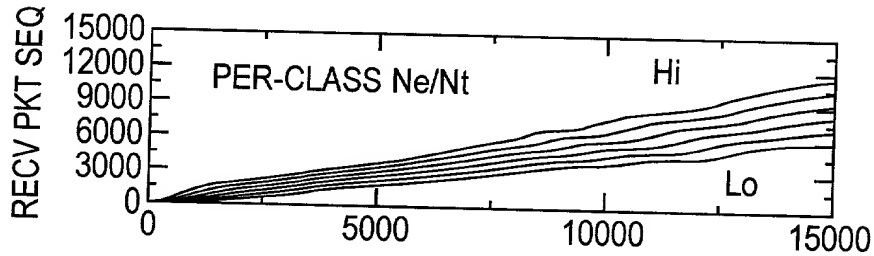


FIG. 15A

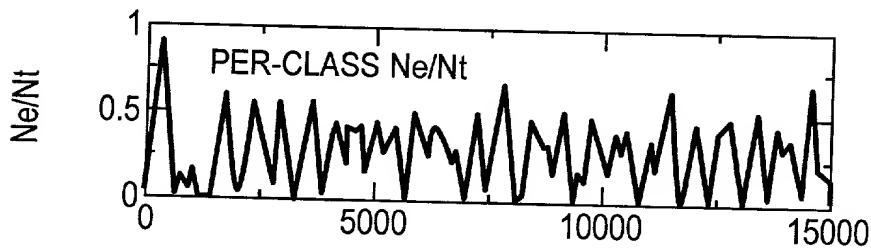


FIG. 15B

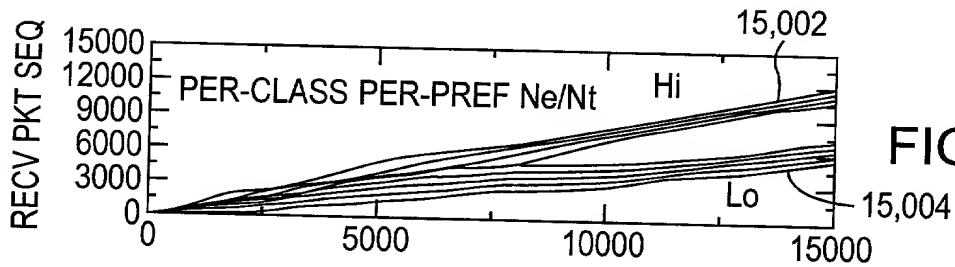


FIG. 15C

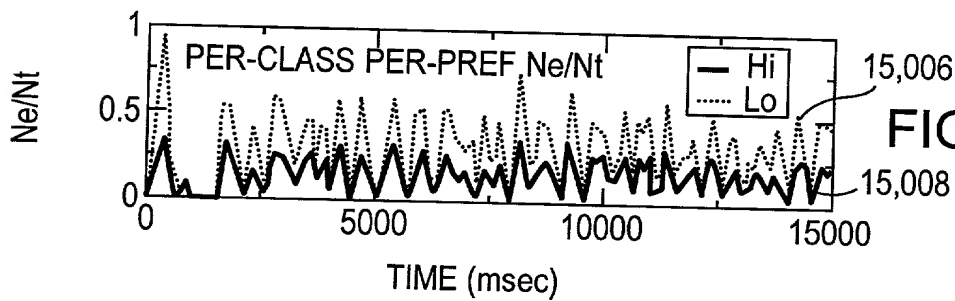


FIG. 15D

PER-CLASS VS. PER-CLASS PER-PREFERENCE Ne/Nt